Remarks

Claims 1-8 are currently pending in this application.

The Examiner rejected applicants' claims 1-4, stating that the claims are anticipated under 35 USC § 102(b). The Examiner cited US Patent No. 5,471,418 to Tanigawa (Tanigawa hereinafter) as the basis for the rejection.

Applicants' invention is an integrated circuit that consists of a semiconductor substrate with semiconductor devices formed therein and thereon, a first wiring layer located over the substrate, a second wiring layer located on the first wiring layer, and a capacitor. The capacitor has metal-based charge-storage electrodes that extend through the entire thickness of the second wiring layer and at least part of the first wiring layer. The wiring layers have interconnect wire embedded therein.

Referring to Figure 1A of applicants' specification, there the applicants illustrate a portion of one integrated circuit (IC) 8. The IC 8 includes a semiconductor substrate 10, semiconductor devices 16, 18 located on the substrate 10, and a protective dielectric layer 14 covering both the semiconductor devices 16, 18 and the substrate 10. Exemplary semiconductor devices 16, 18 include transistors, diodes, and resistors. The IC 8 also includes multiple wiring layers 11-13 located on the layer 14, and an inter-wiring-layer capacitor 20 stacked over the protective layer 14. The inter-wiring-layer capacitor 20 extends through more than one of the wiring layers 12-13. The inter-wiring-layer capacitor 20 is completely disposed in a window formed in the wiring layers 12 and 13.

Referring to FIG. 3 of Tanigawa, the capacitor is clearly not completely disposed in a window formed in insulating layers 6, 8 and 10. The polysilicon storage electrode 11, dielectric layer 12 and opposite electrode 13 are all partially disposed outside the window formed in insulators layers 6, 8 and 10. At column 5, lines 48-58, Tanigawa states that the advantage of its DRAM cell is the fact that the storage electrode 11, the dielectric 12 and the opposite electrode 13 are provided on the third interlayer insulator 10. According to Tanigawa, this provides an advantage, since the thickness of the storage electrode 11 can be made thicker. Thus, Tanigawa teaches away from the present invention by teaching that it is advantageous to have the capacitor partially outside the window in which the capacitor is formed. It is for this reason that applicants' claims 1-4 are neither anticipated by nor obvious from Tanigawa.

The Examiner rejected applicants' claims 5-8 as obvious under 35 USC § 103 (a). The Examiner cited Tanigawa in view of US Patent No. 6,281,535 to Ma et al. (Ma et al. hereinafter) as the basis for his rejection. The references, either alone or in combination, do not describe a capacitor in which the entire capacitor is completely within a window formed in the dielectric layers. Therefore these claims are patentable over this combination of references for the same reason that claim 1 is patentable over this combination of references. That is, by virtue of their dependence on claim 1, claims 5-8 recite a capacitor that is completely within a window formed in the dielectric layers. Such a capacitor is not disclosed in or suggested by Tanigawa in view of Ma et al.

In view of the foregoing arguments and amendments, applicants submit that their claims are in condition for allowance. Favorable action is respectfully requested.

Respectfully submitted,

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RED-LINED VERSION OF AMENDED CLAIM

1. (amended) An integrated circuit, comprising:

a semiconductor substrate including semiconductor devices;

a first wiring layer having an associated thickness being located over the substrate and having interconnect wire embedded therein;

a second wiring layer having an associated thickness being located on the first wiring layer and having interconnect wire embedded therein; and

a capacitor having a first metal-based charge-storage electrode, a second metal-based charge-storage electrode, and a dielectric layer interposed between the charge-storage electrodes, the charge-storage electrodes extending through the thickness of the second wiring layer and at least part of the first wiring layer wherein the capacitor is completely disposed in a window formed in the wiring layer.